What is claimed is:

[Claim 1] A method of making a semiconductor device, comprising the steps of:

forming a source and a drain in a substrate;

forming a gate on the substrate between the source and drain;

forming a substrate contact in electrical contact with the source; and

forming an electrical contact to the source, drain and gate, and the substrate.

[Claim 2] The method of claim 1, further comprising arranging the source and the substrate at substantially the same voltage potential.

[Claim 3] The method of claim 1, further comprising forming the substrate contact in electrical contact with the source.

[Claim 4] The method of claim 3, further comprising forming the substrate contact in direct physical contact with the source.

[Claim 5] The method of claim 1, wherein the substrate contact comprises a p+ region.

[Claim 6] The method of claim 1, wherein the semiconductor device further comprises at least any of an additional source, drain, and gate.

[Claim 7] The method of claim 1, further comprising forming a silicon tab in contact with the substrate contact and forming a silicide layer on a top of the substrate contact.

[Claim 8] The method of claim 1, wherein the substrate contact is formed to partially surround the active region.

[Claim 9] The method of claim 8, wherein the substrate contact is formed to completely surround an active region defined by the drain, source, and gate.

[Claim 10] The method of claim 1, wherein the substrate contact is formed in electrical contact with the source without substantially any non-conductive material therebetween.

[Claim 11] A method of fabricating a device, comprising the steps of:

forming an active region including a source, drain and gate region;

and

forming a collection source configured for shielding electrical noise

external to the active region.

[Claim 12] The method of claim 11, further comprising forming the collection source in electrical contact with the source region.

[Claim 13] The method of claim 11, further comprising forming the collection source in direct physical contact with the source region and either substantially or completely surrounding the active region.

[Claim 14] A semiconductor device, comprising;

a substrate;

a source and a drain arranged within the substrate;

a gate formed on the substrate between the source and drain; and

a substrate contact formed within the substrate in electrical contact with the source.

[Claim 15] The semiconductor device of claim 14, further comprising the substrate contact being configured to shield the semiconductor device from electrical noise.

[Claim 16] The semiconductor device of claim 14, further comprising the substrate contact being in direct physical contact with the source of the semiconductor device.

[Claim 17] The semiconductor device of claim 14, wherein the substrate contact comprises a p+ region.

[Claim 18] The semiconductor device of claim 14, wherein the source comprises a source finger and the substrate contact abuts substantially all of one side of the source finger.

[Claim 19] The semiconductor device of claim 18, comprising at least two source fingers arranged within the substrate, wherein the substrate contact abuts two of the at least two source fingers.

[Claim 20] The semiconductor device of claim 14, wherein the substrate contact comprises a p-type doped silicon tab contacting the source and a silicide layer arranged on a top of the substrate contact.

[Claim 21] A semiconductor device, comprising:

a substrate;

at least two source fingers in the substrate substantially parallel to one another;

at least one drain finger in the substrate between the at least two source fingers;

at least two gate fingers on a top of the substrate, wherein each gate finger is arranged between the at least one drain finger and one source finger of the at least two source fingers; and

a substrate contact within the substrate and adjacent two source fingers of the at least two source fingers configured to shield the semiconductor device from electrical noise.

[Claim 22] The semiconductor device of claim 21, wherein the at least two gate fingers are connected to one another at at least one end with a gate finger bus.

[Claim 23] The semiconductor device of claim 21, wherein the at least two source fingers are connected to one another at at least one end with a source finger bus.

[Claim 24] The semiconductor device of claim 21, further comprising at least two drain fingers, wherein the at least two drain fingers are connected to one another at least at one end with a drain finger bus.

[Claim 25] The semiconductor device of claim 21, wherein the substrate contact electrically contacts two source fingers of the at least two source fingers.

[Claim 26] The semiconductor device of claim 21, further comprising a gate finger bus electrically connecting the at least two gate fingers, wherein:

the at least two source fingers comprise a source metal tab disposed on a top of the substrate and the at least one drain finger comprises a drain metal tab disposed on a top of the substrate,

the gate finger bus is electrically connected to the metal ring,

the only electrical connection to the substrate is through the source metal tab,

the substrate, the at least two source fingers, the at least one drain finger, and the at least two gate fingers are configured to amplify an RF signal.

[Claim 27] The semiconductor region of claim 21, wherein the substrate contact is configured to physically contact all of a side of each of the two source fingers of the at least two source fingers.

[Claim 28] The semiconductor device of claim 21, wherein the substrate contact comprises a p+ region.

[Claim 29] The semiconductor device of claim 21, wherein the substrate contact comprises a p-type doped silicon tab.

[Claim 30] The semiconductor device of claim 21, further comprising a silicide layer arranged on top of the substrate contact.